UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,483	03/31/2004	Gerald L. Dybsetter	15436.366.1	7758

22913 7590 01/07/2010

Workman Nydegger
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, UT 84111

EXAMINER	
PATEL, NIMESH G	
ART UNIT	**PAPER NUMBER**
2111	
MAIL DATE	**DELIVERY MODE**
01/07/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,483	DYBSETTER ET AL.	
	Examiner	Art Unit	
	NIMESH G. PATEL	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 8-10, 12, 13, 23-26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Creedon et al.(US 6,385,669) and Miesterfeld(US 4,706,082).

3. Regarding claim 1, Creedon discloses a system that includes a master component(Figure 1, 10) that is configured to communicate with one or more slave components(Figure 1, 11) over a clock wire(Figure 1, 12) and a data wire(Figure 1, 13), a method for the master component communicating over the data wire while enabling recovery of synchronization between the master component and the one or more slave components, the method comprising the following: determining that an operation is to be performed on a slave component of the one or more slave components(Column 4, Lines 60-61); monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component; detecting at least the predetermined number of consecutive bits of the same binary polarity have occurred on the data wire during the act of monitoring the data wire(Column 4, Lines 62-67); and asserting a frame of a two-wire interface on the data wire in response to the act of detecting that the predetermined number of consecutive bits of the same polarity have occurred on the data wire(Figure 4; Column 5, Line 7).

Creedon does not specifically disclose wherein at least a portion of the consecutive bits do not originate from the master component. However, Miesterfeld discloses a similar bus structure as Creedon. Miesterfeld explains multiple devices can send a logic zero and a logic

one can appear on the bus when the bus is idle or a device is sending a logic one(Column 4, Lines 8-21). It would have been obvious to one of ordinary skill in the art to combine the teachings of Creedon and Miesterfeld so that contention can be avoided and devices are synchronized by making sure the bus is idle before sending data.

4. Regarding claim 2, Creedon discloses a method, wherein the two-wire interface is a guaranteed header two-wire interface(Figure 4).

5. Regarding claim 3, Creedon discloses a method, wherein the two-wire interface is not a guaranteed header two-wire interface(Column 4, Line 67-Column 5, Line 6).

6. Regarding claim 4, Creedon discloses a method, wherein the act of detecting at least the predetermined number of consecutive bits comprises the following: detecting at least the predetermined number of consecutive bits of a logical one(Column 4, Lines 62-67).

7. Regarding claim 5, Creedon discloses a method, wherein the data wire is pulled high when no components are asserting binary values on the data wire(Column 4, Lines 43-44).

8. Regarding claim 8, Creedon discloses a method, further comprising the following: the master component asserting a clock signal on the clock wire during at least some of the act of monitoring the data wire(Column 4, Lines 62-67).

9. Regarding claim 9, Creedon discloses a method, further comprising the following: the master component asserting a voltage level on the data wire during only a portion of the act of monitoring(Column 4, Lines 62-67).

10. Regarding claim 10, Creedon discloses a method, wherein the data wire is pulled high when no components are asserting binary values on the data wire(Column 4, Lines 43-44).

11. Regarding claim 12, Creedon discloses a method, further comprising the following: the master component refraining from asserting a voltage level on the data wire during the act of monitoring(Column 4, Lines 62-67).

12. Regarding claim 13, Creedon discloses a method, wherein the data wire is pulled high when no components are asserting binary values on the data wire(Column 4, Lines 62-67).

13. Regarding claim 23, Creedon discloses a system comprising the following: a master component(Figure 1, 10); a slave component(Figure 1, 11); a clock wire(Figure 1, 14) interconnected between the master component and the slave component; a data wire(Figure 1, 13) interconnected between the master component and the slave component, wherein the master component is configured to perform the following: determining that an operation is to be performed on the slave component(Column 4, Lines 60-61); monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component; detecting at least the predetermined number of consecutive bits of the same binary polarity have occurred on the data wire during the act of monitoring the data wire(Column 4, Lines 62-67); and asserting a frame of a two-wire interface on the data wire in response to the act of detecting that the predetermined number of consecutive bits of the same polarity have occurred on the data wire(Figure 4; Column 5, Line 7).

Creedon does not specifically disclose wherein at least a portion of the consecutive bits do not originate from the master component. However, Miesterfeld discloses a similar bus structure as Creedon. Miesterfeld explains multiple devices can send a logic zero and a logic one can appear on the bus when the bus is idle or a device is sending a logic one(Column 4, Lines 8-21). It would have been obvious to one of ordinary skill in the art to combine the teachings of Creedon and Miesterfeld so that contention can be avoided by making sure the bus is idle before sending data.

14. Regarding claim 24, Creedon discloses a system, wherein the two-wire interface is a guaranteed header two-wire interface(Figure 4).

15. Regarding claim 25, Creedon discloses a system, wherein the two-wire interface is not a guaranteed header two-wire interface(Column 4, Line 67-Column 5, Line 6).

16. Regarding claim 26, Creedon discloses a system, wherein the data wire is pulled high when no components are asserting binary values on the data wire(Column 4, Lines 43-44).

17. Regarding claim 28, Creedon discloses a master component that is configured to do the following when coupled to a slave component via a clock wire and a data wire: determining that an operation is to be performed on the slave component; monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component(Column 4, Lines 60-61); detecting at least the predetermined number of consecutive bits of the same binary polarity have occurred on the data wire during the act of monitoring the data wire(Column 4, Lines 62-67); and asserting a frame of a two-wire interface on the data wire in response to the act of detecting that the predetermined number of consecutive bits of the same polarity have occurred on the data wire(Figure 4; Column 5, Line 7).

Creedon does not specifically disclose wherein at least a portion of the consecutive bits do not originate from the master component. However, Miesterfeld discloses a similar bus structure as Creedon. Miesterfeld explains multiple devices can send a logic zero and a logic one can appear on the bus when the bus is idle or a device is sending a logic one(Column 4, Lines 8-21). It would have been obvious to one of ordinary skill in the art to combine the teachings of Creedon and Miesterfeld so that contention can be avoided by making sure the bus is idle before sending data.

18. Regarding claim 29, Creedon discloses a master component, wherein the two-wire interface is a guaranteed header two-wire interface(Figure 4).

19. Regarding claim 30, Creedon discloses a master component, wherein the two-wire interface is not a guaranteed header two-wire interface(Column 4, Line 67-Column 5, Line 6).

20. Claims 6, 7, 11, 14-22 and 31-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Creedon, Miesterfeld and what is well known in the art.

21. Regarding claims 6 and 27, Creedon does not specifically disclose a system and method, wherein detecting at least the predetermined number of consecutive bits of a logical zero. However, official notice is being taken that pull-down resistors are well known in the art and easily replace pull up resistors when a default zero logic is desired instead of logic one(see Whitney et al.(US2003/0025587)(Paragraph 69)). It would have been obvious to one of ordinary skill in the art to replace the pull-up resistor with a pull-down resistor so the master can detect logical zeros as the preamble.

22. Regarding claim 7, a pull down resistor, as explained above, would pull the data wire low if no components are asserting binary values(see Whitney et al.(US2003/0025587)(Paragraph 69)).

23. Regarding claims 11 and 14, Creedon does not specifically disclose a method, wherein the data wire is pulled low when no components are asserting binary values on the data wire. However, official notice is being taken that pull-down resistors are well known in the art and easily replace pull up resistors when a default zero logic is desired instead of logic one(see Whitney et al.(US2003/0025587)(Paragraph 69)). It would have been obvious to one of ordinary skill in the art to replace the pull-up resistor with a pull-down resistor so that the data wire is pulled low when no components are asserting binary values on the data wire.

24. Regarding claims 15-18 Creedon discloses an MDIO interface but does not specifically disclose a method, wherein, determining that a read or write operation is to be performed with an extended or shorter address as compared to other frames communicated over the data wire.

However, official notice is being taken components having different size addresses in the MDIO interface is well known in the art(see IEEE 802.3 standard, Section 45.1 Overview). It would have been obvious to one of ordinary skill in the art to determine a read or write operation is to be performed with an extended or shorter address as compared to other frames since this give the ability to access more device register while retaining logical compatibility with the MDIO interface defined in Clause 22 of the IEEE 802.3 standard.

25. Regarding claims 19 and 20, Creedon does not specifically disclose a method, wherein determining that a read or write operation is to be performed with cyclic redundancy checking over the data wire. However, official notice is being taken CRC checking is well known in the art(see CRC definition submitted with this office action). It would have been obvious to one of ordinary skill in the art to use CRC checking to ensure there are no errors during transmission.

26. Regarding claims 21 and 22, Creedon does not specifically disclose a method, wherein determining that a read or write operation is to be performed with acknowledgements over the data wire. However, official notice is being taken acknowledgements are well known in the art(see ACK definition submitted with this office action). It would have been obvious to one of ordinary skill in the art to use acknowledgements since this would ensure the master and slave receiving data properly.

27. Regarding claims 31-39, Creedon does not specifically disclose a master component, wherein the master component is implemented in a laser transmitter/receiver and the various types of laser transmitter/receivers. However, official notice is being taken, that it is well known in the art to use various types of laser transmitter/receivers(see Nelson et al.(US2005/0111845)(Paragraph 78). It would have been obvious to use any types of laser transmitter/receivers to increase compatibility and realize various data rates applicable to each specific situation or environment.

28. Regarding claim 40, Creedon does not specifically disclose a master component in accordance with Claim 1, further comprising the following: interspersing a bit at a guaranteed minimum frequency among data transmitted on the data wire, wherein the interspersed bit is of a polarity opposite that of the detected predetermined number of consecutive bits. However, official notice is being taken that this is well known in the art as zero-bit insertion. As evidence, a definition of bit stuffing is being supplied. Bit stuffing is used to prevent data being interpreted as control information. It would have been obvious to one of ordinary skill in the art to use zero stuffing since this will prevent consecutive bits of data being confused with the preamble of consecutive bits.

Response to Arguments

29. Applicant's arguments filed October 9, 2009 have been fully considered but they are not persuasive.

30. In response to applicant's argument that Creedon and Meisterfield cannot be combined, Examiner respectfully disagrees. Creedon discloses a bus structure that includes a bus, where when idle, a logic one appears on the bus(Figure 2, Pull-up resistor 21 causes the bus to be a logic one when idle). Creedon further discloses a preamble of 32 consecutive logic one bits to synchronize the devices(Column 4, Lines 62-67), Creedon does not specifically go into details various scenarios when a device is transmitting on the bus. One of ordinary skill in the art would look for a similar bus structure and find Meisterfield. Meisterfield also discloses a bus structure that includes a bus, where when idle, a logic one appears on the bus(Column 4, Lines 8-21). Meisterfield explains that a logic one appears on the bus if the bus is idle or when a device is transmitting a logic one. Meisterfield further explains that the only way a logic zero appears on the bus is when a device is transmitting a zero. As explained earlier, Creedon uses a similar bus

structure and uses a preamble of 32 consecutive logic one bits to synchronize the devices. One of ordinary skill in art would recognize how important is to have 32 consecutive logic ones to appear the bus so that the devices a can be synchronized. As explained by Meisterfield, a logic one will appear on the bus if any of the devices are transmitting a logic one or the bus is idle and if any device transmits a logic zero, a logic zero will appear on the bus. As admitted by Applicant, Meisterfield relates to contention(see abstract) and has a similar bus structure to Creedon. One of ordinary skill in the art would be motivated to combine the teachings of Creedon and Meisterfield so that contention can be avoided and devices are synchronized by making sure the bus is idle before sending data.

31. Therefore, Applicant's arguments are not persuasive.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIMESH G. PATEL whose telephone number is (571)272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rinehart H. Mark can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nimesh G Patel/
Examiner, Art Unit 2111

/Mark Rinehart/
Supervisory Patent Examiner, Art Unit 2111